



Attorney's Docket No.: 42P17292

Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re Application of:

Brian Doyle et al

U.S. Serial No: 10/816,232

Filed: March 31, 2004

For: SEMICONDUCTOR DEVICE
HAVING A Laterally Modulated
Gate Workfunction and Method
of Fabrication

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Examiner: Wojciechowicz, Edward J

Art Unit: 2815

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1/9/06

Date

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Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

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01/12/2006 HDESTA1 00000021 10816232

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_____ 37 C.F.R. §1.97(b).

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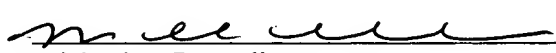
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If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 1/9/06, 2005 
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(use as many sheets as necessary)

Application Number	10/816,232
Filing Date	3/31/2004
First Named Inventor:	Brian Doyle
Art Unit	2815
Examiner Name	Wojciechowicz, Edward J

Sheet	1	of	2	Attorney Docket Number	42P17292
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Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				
		JP 62073668	04/04/1987	Yamamoto		
		JP 05226362	9/3/1993	Matshuhashi		
		JP 05243564	9/21/1993	Yoshihiro		
		EP 0856892 A2	8/5/1998	Okihara et al.		
		WO 0077828 A2	12/21/2000	Stolk et al.		

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Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Application Number	10/816,232
				Filing Date	3/31/2004
				First Named Inventor:	Brian Doyle
				Art Unit	2815
				Examiner Name	Wojciechowicz, Edward J
Sheet 2	of	2	Attorney Docket Number	42P17292	
NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published			T ²
		International Searching Authority Report (ISR) PCT/US05/010506 and Written Opinion of ISA mailed 11/30/2005.			
		ANONYMOUS: "MOS Transistor with Engineered Metal Electrodes, including fabrication process." Research Disclosure, Kenneth Mason Publications, Westbourne, GB, vol. 438, no. 1, Oct. 2000.			
		FROHLICH K ET AL: "Ru and RuO2 gate electrodes for advanced CMOS technology" Materials Science and Engineering B, Elsevier Sequoia, Lausanne, CH, vol. 109, no. 1-3, 5 March 2004, pages 117-121.			
		LANDER R J P ET AL: "A Tuneable Metal Gate Work Function Using Solid State Diffusion of Nitrogen," Proceedings of the 32 nd European Solid-State Device Research Conference, Univ. of Bologna, Bologna, Italy, 2002, pp 103-106.			
		LIN R ET AL, "An Adjustable Work Function Technology Using Mo Gate for CMOS Devices," IEEE Electron Device Letters, IEEE Inc., New York, vol. 23, no. 1, Jan 2002, pp.49-51.			

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